Exhibit "A"

Invention disclosure submission
Complete all sections and send to the Nortel Patent Dept at:
OTTAWA, Canada: Patent Dept., 0265, NTPAT
or HARLOW, UK: Patent Dept., HAL05
or RICHARDSON, USA: Patent Dept., Mail Stop C-0419, RICH1

No. TW0007
Rec'd. 17 Mar 98
Attny/Agent

NORTEL
NORTHERN TELECOM

Invention Title

Method for Sending ATM Cells Across PCI to PCI Bridges With Small Buffers From The Secondary to Primary Side

Correspondence will be directed to the first-named inventor only.

(1) Full legal name of first inventor (include middle initial)

Wegner Norbert

Name usually known as:
Norbert

Global ID

Residence and post office address if different

Phone	Location	Department	Mailstop	Occupation	Fax
	WINNIPE	CPE	n/a		

Signature | Date

Citizen of
CANADA

(2) Name of supervisor or divisional head

Bernard Brown

Name of AVP Reported to:

Doug Smith

Signature | Date

(5) Project Number

n/a

(6) Indicate your LOB

Wireless Networks

If Advanced Technology, please indicate which group.

Please Make a Selection

Technical field

(3) Date of first written description.

Has this invention been discussed with others? If so, please complete.

Outside Nortel To Whom?
When?

Was there a Non-Disclosure Agreement in place?

Inside Nortel To Whom?
When?

Key words for searching

Are you aware of any imminent future disclosures? Please detail.

(4) Which products will use this invention?

(7) Is the invention relevant to a Standards activity?

If so give details:

(8) Does this invention origin from any arrangement involving any external organization? no

Organization

Contract no.

TECHNICAL INFORMATION No. TW0007

(a) Brief description of the invention

Refer to documentation submitted to JP Fortin during his March 12/98 visit.

(b) What is the problem solved by the invention?

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TECHNICAL INFORMATION (continued) No. TW0007

(c) What other solutions have been tried and what were their shortcomings?

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(e) What is the commercial value of the invention to Nortel and Nortel's major competitors? (see guidelines)

This method allows the following: use of bridges to expand slot count in a CPCI chassis, use of a PCI bus for both control and data transfer, use of a single receive buffer on target cards.

The Compact PCI spec. limits the number of slots per PCI bus to 8 including the processor board. This leaves 7 useable expansion slots. With 2 bridges in a chassis we can add an additional 2 PCI busses to allow 19 expansion slots in a chassis.

Additional Inventors / Contractor Information

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Global ID

Residence address (and post office address if different)

Phone	Location	Department	Mailstop	Occupation	Fax
	WINNIPEG	CPE	n/a		

Signature | Date

Citizen of
CANADA

Contractor Information

Agency worked for

Non disclosure agreement with Nortel

Exhibit B of the Master Services agreement with your agency

Any other agreement(s) with your agency.

Please specify

(1) Full legal name of 2nd inventor (include middle initial)

Peter A. ~~We attached~~ tbd

Residence address (and post office address if different)
To be sent later

Phone	Location	Department	Mailstop	Occupation	Fax
	WINNIPE	NNE	n/a		

Signature | Date

Citizen of
UKRAINE

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(1) Full legal name of 4th inventor (include middle initial)

Residence address (and post office address if different)

Phone	Location	Department	Mailstop	Occupation	Fax

Signature | Date

Citizen of

Contractor Information

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What are the specific elements or steps that solved the problem and how do they do it?

ATM cells are kept intact while crossing the bridge by preventing disconnects from happening in the middle of the burst of an ATM cell to the bridge. This is done by ensuring there is enough room in the buffer to receive a complete ATM cell. If there isn't enough room the arbiter inhibits grants to all initiators on the bus.

What is the commercial value of the invention to Nortel and Nortel's major competitors?

This method allows the following: use of bridges to expand slot count in a CPCI chassis, use of a PCI bus for both control and data transfer, use of a single receive buffer on target cards.

The Compact PCI spec. limits the number of slots per PCI bus to 8 including the processor board. This leaves 7 useable expansion slots. With 2 bridges in a chassis we can add an additional 2 PCI busses to allow 19 expansion slots in a chassis.

Sending ATM Cells Across PCI to PCI Bridges With Small Buffers From The Secondary to Primary Side

Problem:

Nortel –BWA is using the PCI bus as a medium to transfer ATM cells between cards in a chassis based Compact PCI product. Since the Compact PCI bus is limited to 8 loads per bus segment PCI to PCI bridges are used to extend the number of slots that can be supported in a single chassis. In order to maximize the bandwidth of the PCI bus, all cards in the system transfer their outgoing ATM cells by performing a write burst of a 14 Dword ATM cell to a preprogrammed target address. Using writes to transfer data allows write posting across PCI to PCI bridges which maximizes bandwidth utilization. If the target address is on a different bus segment than the initiator, the burst will be write posted into the bridge's buffer. If an initiator is bursting an ATM cell across the bridge and the bridge buffer fills up, then the bridge will do a target disconnect even if the ATM cell has not been completely transferred. The arbiter will grant the bus to the next initiator which will write a complete ATM cell over top of the partial ATM cell that is already in the buffer. The initiator that was disconnected will finish sending its ATM cell when it is next granted the bus. If all of the cells crossing the bridge were to the same target address, the cells will be corrupted when they arrive at the target because of the disconnect that happened while crossing the bridge.

Certain cards in the system, such as modems and cell multiplexers, will have multiple cards writing to a single FIFO target location on that card. In order for these cards to operate properly the 14 DWord bursts must be written into the FIFO as complete cells and not as partial cells. i.e. the ATM cells must arrive in their entirety and not be broken up.

A summary of the problem is that target disconnects must be prevented when data from multiple initiators intended for a single target address crosses a PCI to PCI bridge to ensure that ATM cells arrive intact.

Solution:

The CPCI architecture is as shown in figure 1. Arbitration on Bus 1 is controlled by the Host to PCI bridge that physically resides on the host CPU. Arbitration on Busses 2 and 3 is controlled by the PCI to PCI bridge connected to them. The following assumptions are made when using this architecture:

- all cards that have a target address on them that will be simultaneously written to by multiple initiators must be on the Bus 1.
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Based on these assumptions, disconnects must only be prevented when data is being written from busses 2 or 3 to bus 1. This is because disconnects are only a problem when multiple initiators are writing to a single target which by definition is on bus 1.

Disconnects on busses 2 and 3 are avoided by preventing any of the cards on the secondary bus from being granted the bus when there isn't enough room in the bridge buffer for a complete ATM cell. A counter exists on the PCI to PCI bridge module that is incremented when a card on its secondary side starts a write transaction to the bridge. The write may be a single word or a multi DWord burst and will be referred to a data unit. The counter is decremented when the bridge successfully completes a write transaction on its primary side. The counter is not decremented if the bridge gets a target disconnect since this indicates that the data unit was not completely sent. If the counter value is equal to the maximum number of data units that the secondary to primary buffer on the bridge can hold, then the arbitration on the secondary bus is parked and the bus is granted to the bridge whether it is requesting or not. Arbitration is not affected when the count value is less than this maximum value. The size of the data unit is assumed to the maximum size of a burst which is 14 DWords.

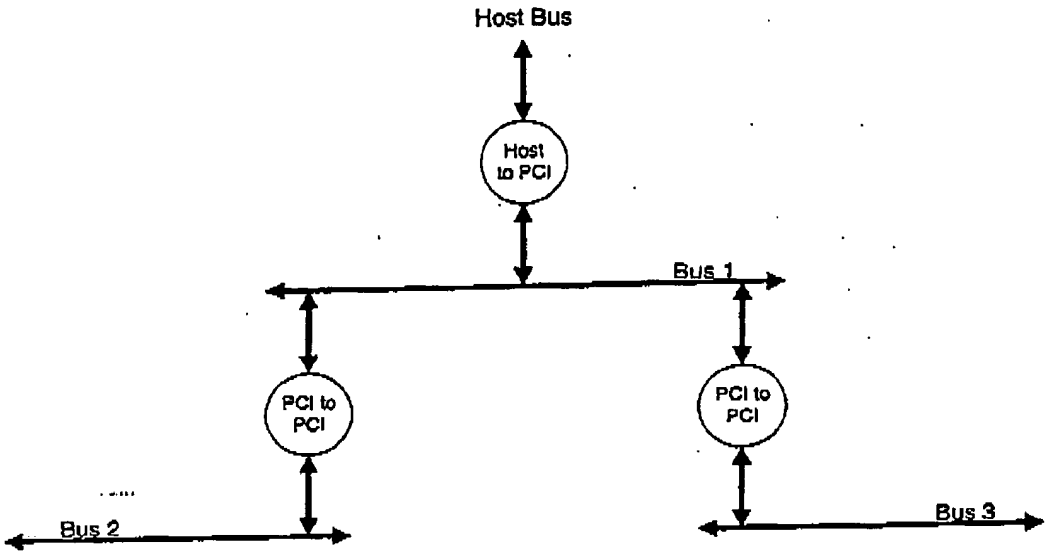

Figure 1 - Nortel – BWA Compact PCI Architecture

Counting data units requires only a small counter and thus minimal hardware resources. The limitation to this method is that it assumes that all data units are the same size, which is generally the case. If the size of the data units varies, the buffer is inefficiently utilized. If the size of the data units varies an extension of this method is to count DWords instead of data units and to disable the grants to the secondary bus if there is not enough room for the maximum size of a burst. This requires more hardware to implement.

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Additional Inventors / Contractor Information

No. TW000

(1) Full legal name of first inventor (include middle initial)				Residence address (and post office address if different)	
Wegner Norbert Global ID					
Phone	Location WINNIPEG	Department CPE	Mailstop n/a	Occupation	Fax
Signature		Date		Citizen of CANADA	
Contractor Information Agency worked for Non disclosure agreement with Nortel Exhibit B of the Master Services agreement with your agency				Any other agreement(s) with your agency. Please specify	

(1) Full legal name of 2nd inventor (include middle initial)				Residence address (and post office address if different)	
Peter A. as attached tbd				To be sent later	
Phone	Location WINNIPE	Department NNE	Mailstop n/a	Occupation	Fax
Signature		Date		Citizen of UKRAINE	
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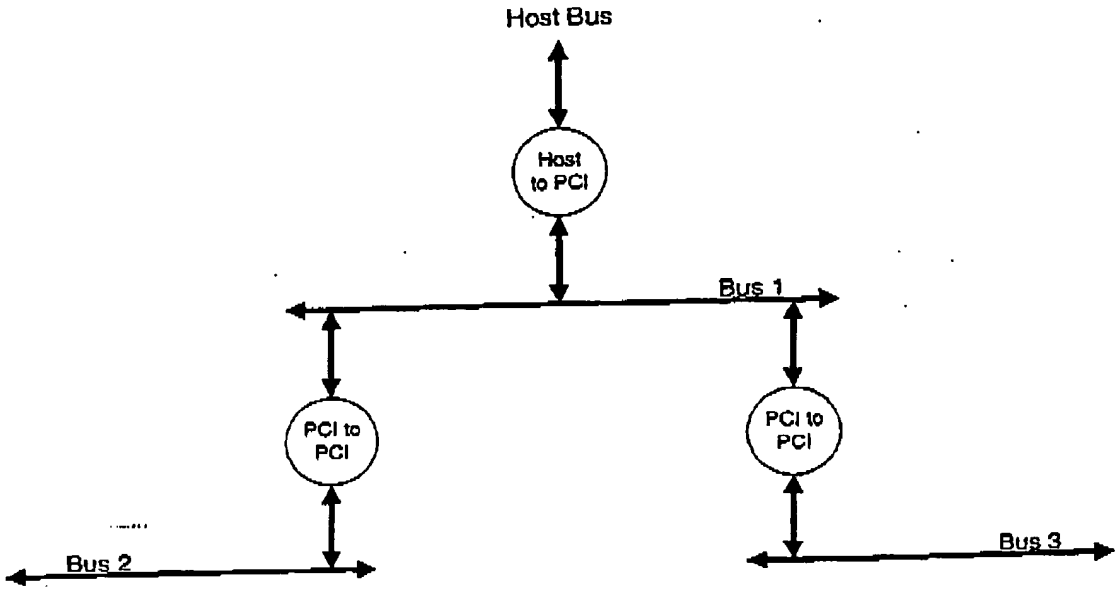

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